



Powerlink Industrial Networking

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Introduction

Ethernet POWERLINK is an open network protocol extended from the Ethernet standard. It offers real-time deterministic bus access for automation systems. It is suitable for applications with hard real-time requirements in a range of microseconds or guaranteed transmission of packet data within well defined time period.

Ethernet POWERLINK is patent-free technology developed by the Ethernet Powerlink Standardization Group. Ethernet POWERLINK is essentially CANopen over Ethernet and it essentially works over standard Ethernet cables.

Ethernet POWERLINK achieves real-time deterministic data transfer by regulated timing of data exchange. Time-slice procedure is employed in the system which prompts every network node to send within a clearly defined span of time. All nodes on the network only reports when they are called upon and observe proper sequence and pre-determined period or time-slice for sending.

The Ethernet POWERLINK website is www.ethernet-powerlink.org

Avnet Design Services has completely implemented a Controlled Node solution on a Xilinx Spartan-3 FPGA. Compared to an MCU based implementation, this FPGA based solution much more compact and integrated. Most essentially this is considered a hardware + software implementation and thus its performance surpasses a full software based MCU solution. It is able to achieve a much higher system real-time response requirement.

As well, since it is FPGA based, it can be upgraded in the field to support difference controlled I/O devices and interfaces.

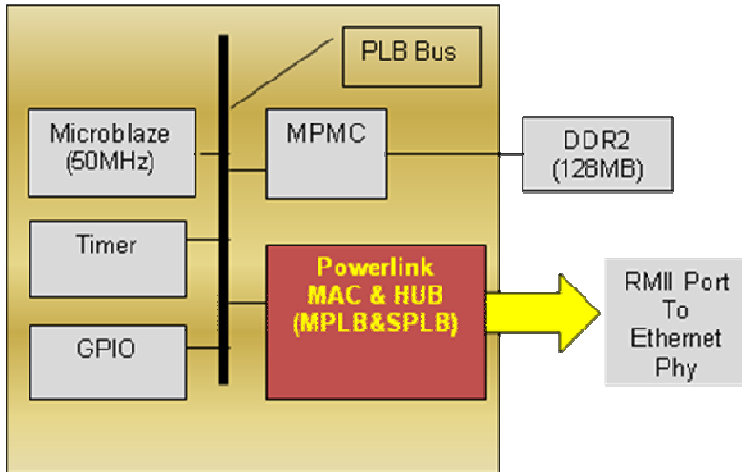
Ethernet POWERLINK Controlled Node on Xilinx FPGA

This is a comprehensive implementation of the POWERLINK **Controlled Node** complete with hardware platform. The solution is completely enabled on the Xilinx Spartan-3 FPGA XC3S700A which internally implements the following modules:

- Microblaze (soft MCU core) : POWERLINK software protocol stack
- POWERLINK optimized Ethernet MAC & includes Ethernet HUB
- Auto-response implementation with the Ethernet MAC
- DDR2 memory controller
- Timer
- UART
- General Purpose programmable I/O

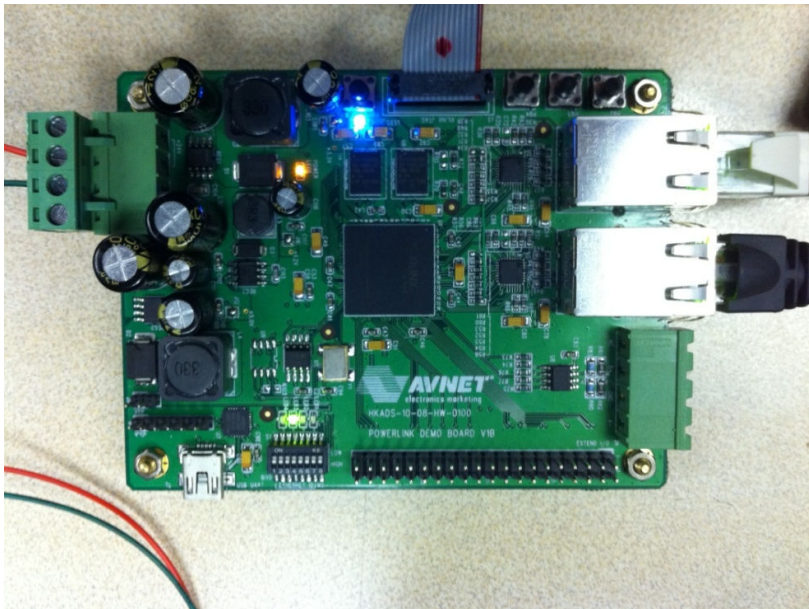
The complete package is made available as an EDK version 12.3 project package with the SDK for the protocol stack implementation.

Following is a general overview of the FPGA system block diagram.



Hardware Board Features

- Xilinx Spartan-3 XC3S700A FPGA
- Two 10/100 Ethernet Phy. Interfaces
- 2 x DDR2 x 64Mb
- USB to UART (CP2103) interface
- 12V power supply
- 50Mhz clock oscillator
- 8 General Purpose DIP switches
- 4 General Purpose LED indicators



Windows XP GUI for Quick Start

A simple Windows XP application is available for a Quick Start setup to emulate a POWERLINK Managing Node.

