Xilinx Spartan-6 Powerlink Industrial Networking

Document
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1. Introduction

Ethernet POWERLINK is an open network protocol extended from the Ethernet standard. It offers real-time deterministic bus access for automation systems. It is suitable for applications with hard real-time requirements in a range of microseconds or guaranteed transmission of packet data within well defined time period.

Ethernet POWERLINK is patent-free technology developed by the Ethernet Powerlink Standardization Group. Ethernet POWERLINK is essentially CANopen over Ethernet and it essentially works over standard Ethernet cables.

Ethernet POWERLINK achieves real-time deterministic data transfer by regulated timing of data exchange. Time-slice procedure is employed in the system which prompts every network node to send within a clearly defined span of time. All nodes on the network only report when they are called upon and observe proper sequence and pre-determined period or time-slice for sending.

The Ethernet POWERLINK website is www.ethernet-powerlink.org

Avnet Design Services has completely implemented a Controlled Node solution on a Xilinx Spartan-3 & Spartan-6 FPGA. Compared to an MCU based implementation, this FPGA based solution much more compact and integrated. Most essentially this is considered a hardware + software implementation and thus its performance surpasses a full software based MCU solution. It is able to achieve a much higher system real-time response requirement.

As well, since it is FPGA based, it can be upgraded in the field to support different controlled I/O devices and interfaces.

2. Hardware Demo Board Features

FPGA
- Spartan-6 XC6SLX16-CSG324C-2

Configuration
- Onboard configuration circuitry (Xilinx JTAG Cable connector / Digilent Inc. JTAG SMT1 module)
- Quad SPI Flash 64 Mb

Memory
- DDR2 x 1: 512Mb (32M x 16)
- SRAM x 2: 8Mb (256K x 32)

Communication
- 10/100 Ethernet PHY, National Semiconductor DP83640 x 2
- USB to RS232 serial(UART) bridge
- Powerlink PDI interface

Clocking
- 50MHz oscillator (Single-Ended)

Display
- 8 User LEDs

Control
- 4 Push buttons
- 4 Positions DIP switch
- 2 Rotary encoders (4 bit each) for Node ID
Power Management

- 9 ~ 24VDC input DC-DC to 5V
- 5V DC-DC to 3.3V, 1.8V, 1.2V & 0.9V

Block Diagram

- 512Mb DDR2, 256K x 16 SRAM x 2
- 4 x Push Buttons, 4 Positions DIP Switch, 2 x 4-bit Rotary Encoders
- Xilinx JTAG Connector / Digilent Inc SMT1, 64Mb QSPI Flash
- 5V, 3.3V, 1.8V, 1.2V and 0.9V DC-DC
- 50 MHz Oscillator
- 8 x User LEDs
- Spartan6 XC6SLX16 CSG324-2
- DPI Interface
- 2 x 10/100 Ethernet PHY
- USB-RS232 Bridge
- 4 x 10/100 Ethernet PHY
3. Design Features
This is a comprehensive implementation of the POWERLINK Controlled Node complete with hardware platform. The solution is completely enabled on the Xilinx Spartan-6 FPGA XC6SLX16 which internally implements the following modules:

- Microblaze (soft MCU core): POWERLINK software protocol stack
- POWERLINK optimized Ethernet MAC & includes Ethernet HUB
- Auto-response implementation with the Ethernet MAC
- SRAM memory controller
- DDR2 memory controller
- Timer
- UART
- General purpose programmable I/O

The complete package is made available as an EDK version 12.3 project package with the SDK for the protocol stack implementation.

The following figure illustrates the EDK design that serves to demonstrate the Powerlink protocol.
4. Windows XP GUI for Quick Start

A simple Windows XP application is available for a Quick Start setup to emulate a Powerlink Managing Node.

Remark:
- The MN application relies on Windows timer to generate Powerlink cycle. However, this timer is not accurate enough for our Powerlink demo. Therefore, you may find Powerlink cycle broken occasionally. This isn’t the issue on the CN.

5. Reference

- Powerlink Specifications
  www.ethernet-powerlink.org

- Powerlink Stack source code
  http://sourceforge.net/projects/openpowerlink

- All Spartan-6 Documentation
  http://www.xilinx.com/support/documentation/spartan-6.htm
### Revision History

The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Revision</th>
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<td>10 Jan 2012</td>
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